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Accelerating Artificial Intelligence-enabled System-on-Chip Designs

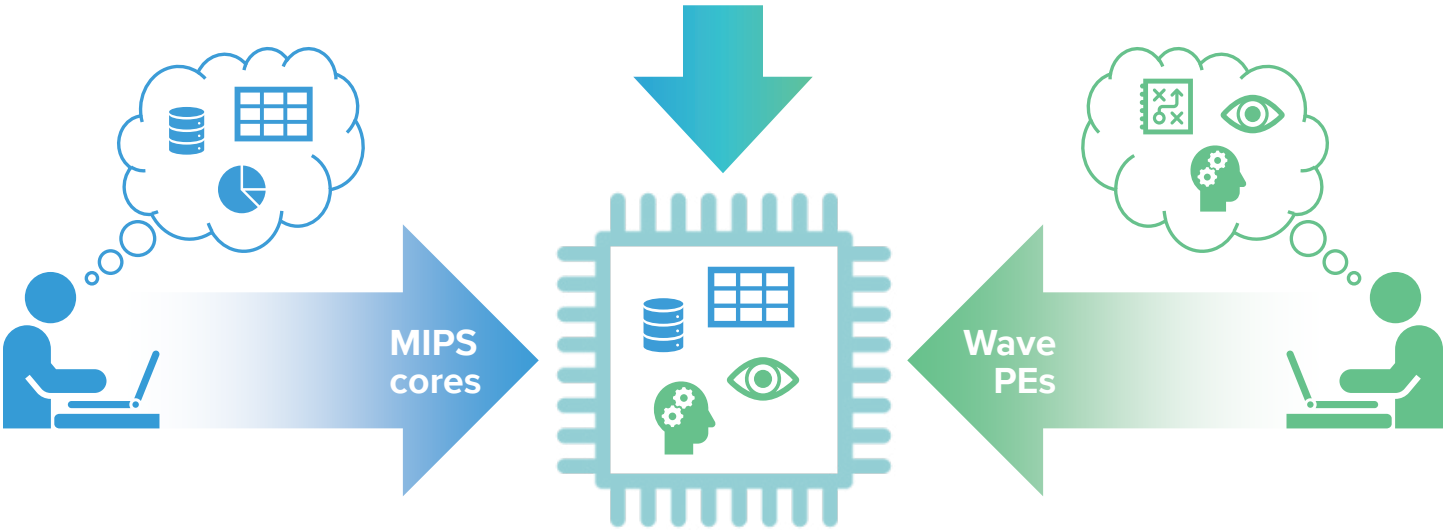
Application-enabling CPU Cores

- 32 & 64-bit RISC architecture
- Silicon-proven
- Scalable through multiple cores or threads
- TensorFlow & Linux “host,” with AI features

AI-native DPU Cores

- 8-to-64-bit Dataflow Architecture
- Silicon-proven
- Scalable CGRA fabric
- CPU-less acceleration of dataflow graphs

AI-infused IP



High Scalability, Performance, and Efficiency, with Low Latency

- **User Application**
- **AI Session Manager**
- **OS/Linux/RTOS**

- **Native dataflow graph execution**
- **Reprogrammable AI Agents**
- **Neural Network**